REMARKS

By the present amendment claims 1, 7 and 8 have been amended to clarify the invention.

New claims 11-14 have been added. Claim 10 has been cancelled without prejudice or disclaimer to the subject matter contained therein.

Claims 1-9 and 11-14 remain pending in the application.

In the Office Action, the Examiner objected to the drawings.

Claims 7-8 were rejected under 35 U.S.C. § 112, second paragraph.

Claims 1-3 and 6 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Publication Number 2002/0050972 A1 to Udo et al.

Claims 4-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over Udo et al.

Claims 7-8 and 10 were rejected under 35 U.S.C. §103(a) as being unpatentable over Udo et al. in view of Japanese Patent Number 09-212137 to Masami et al.

In view of the arguments that follow, Applicants respectfully traverse the Examiner's rejection of claims 1-10.

By this amendment, Applicants have amended claims 1, 7, and 8 to more appropriately recite the present invention. It is respectfully submitted that these amendments are being made without conceding the propriety of the Examiner's rejection but merely to timely advance prosecution of the present application.

Rejections Under 35 U.S.C. §112, second paragraph

The Examiner rejected claims 7-8 under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner asserted that the limitation of "with respect to both a data signal line to be scanned first and a data signal line to be scanned next" in the claim was not clear as to how data lines could be scanned.

Applicants respectfully submit that claims 7 and 8 have been amended to overcome the rejection.

Rejection Under 35 U.S.C. § 102(b)

The Examiner rejected claims 1-3 and 6 under 35 U.S.C. §102(e) as being anticipated by Udo et al. The rejection is respectfully traversed.

Applicants amended claim 1, recites an image display device, comprising: a plurality of scanning signal lines and a plurality of data signal lines which cross each other; an electro-optical element, and a switching element and a pixel capacitor which correspond to said electro-optical element, said electro-optical element and corresponding switching element and pixel capacitor being provided in each pixel region surrounded by adjacent two of said plurality of scanning signal lines and adjacent two of said plurality of data signal lines; a data signal line driving circuit for outputting voltages for display in mutually reverse polarities with respect to a pair of adjacent pixels in a

direction of the data signal lines; and short-circuit means for short-circuiting respective pixel capacitors of said pair of adjacent pixels before applying the voltages for display to a pixel to be scanned first of the pair of adjacent pixels in the direction of the data signal lines when scanning in switching polarities of the voltages for display.

The Examiner alleged that Udo et al. teach the recitations of claim 1. Specifically, the Examiner alleged that Udo et al. teach a short-circuit means for short-circuiting respective pixel capacitors of pair of adjacent pixels (Fig. 9, references D1-D2 and S1; page 1, paragraph 0010) in non-selection period directly before a selection-scanning period of a target scanning signal line when scanning by switching polarities of the voltages (Figs. 8-9, references D1-D2 and S1; page 1, paragraphs 0007-0011) for gradation display (page 1, paragraph 0002).

Applicants respectfully submit that the Udo et al. patent does not disclose or teach a "short-circuit means for short-circuiting respective pixel capacitors of said pair of adjacent pixels before applying the voltages for display to a pixel to be scanned first of the pair of adjacent pixels in the direction of the data signal lines when scanning in switching polarities of the voltages for display," as recited in claim 1.

Udo et al. merely disclose a liquid crystal display (LCD) with a pair of opposed glass substrates and a gap therebetween filled with a liquid crystal and sealed. Pixel electrodes are arranged in a matrix on one of the glass substrates, thin film transistors are formed in the respective pixels, scan bus lines are formed and data bus lines are formed of the thin film transistors. The thin film transistor is connected between the pixel electrode and the data bus line, the gate of the thin film transistor is connected to the scan bus line and a common potential (VCOM) is applied to an opposite electrode of the liquid crystal pixel.

Udo et al. further discloses short-circuiting switches in the data driver that are connected between one of every other adjacent data bus lines concerned with the same display color. A control circuit puts outputs of voltage buffer amplifiers in the data driver into a high impedance state during successive horizontal blanking periods, and during each period, turns on all the short-circuiting switches. Once the short-circuiting switches are turned on, potentials of the data bus lines are rendered to be almost equal to the common potential (VCOM), currents consumed in the voltage buffer amplifiers are reduced to almost a half, and a circuit area of the data driver is reduced enabling higher data bus line density.

The short-circuit switches located in the data driver that are connected between every other adjacent data bus lines of Udo et al. do not short circuit "pixel capacitors in the liquid crystal panel of said pair of adjacent pixels." The short-circuit switches of Udo et al. simply allow the potential of the data bus lines to become nearly equal to the common potential in order to reduce the current in the voltage buffer amplifiers. Moreover, there is nothing in Udo et al. that disclose or teach a ""short-circuit means for short-circuiting respective pixel capacitors of said pair of adjacent pixels before applying the voltages for display to a pixel to be scanned first of the pair of adjacent pixels in the direction of the data signal lines when scanning in switching polarities of the voltages for display." Udo merely discloses the technique of short-circuiting between data bus lines by setting ON a short-circuit switching element provided in the voltage buffer amplifier in a high impedance state of an output of a voltage buffer amplifier in a horizontal blanking period. Specifically, Udo et al. discloses the structure of connecting the adjacent data bus lines by the short-circuit switching element (Fig. 9) and the structure for connecting by the short-circuit

switch, adjacent data bus lines with regard to the same display color (Fig. 3 and Fig. 4). However, there is no teaching in Udo et al. that is directed to the short-circuit means of the present invention.

Applicants respectfully submit that Udo et al. do not disclose or teach the claimed invention of claim 1, and the rejection of claim 1 should be withdrawn. Dependent claims 2-6, are allowable for at least the same reasons with regards to independent claim 1 and based on their dependency.

Rejection Under 35 U.S.C. § 103

The Examiner rejected claims 7-8 and 10 under 35 U.S.C. §103(a) as being unpatentable over Udo et al. in view of Masami et al. The rejection is respectfully traversed.

With respect to claim 7, the Examiner alleged that Udo et al. teaches an image display device, comprising: a plurality of scanning lines and a plurality of data lines which cross each other; an electro-optical element, and a switching element and a pixel capacitor being provided in each pixel region surrounding by adjacent two of said plurality of scanning signal lines and adjacent two of said data signal lines; a data signal line driving circuit for outputting voltages for gradation display in mutually reverse polarities with respect to a pair of adjacent pixels in a direction of said data signal line.

The Examiner admitted that Udo et al. do not show separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving

circuit, separation means being provided between an output stage of data signal line driving circuit and data signal line and scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair.

To cure the deficiencies of Udo et al., the Examiner alleged that Masami et al. teach separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning live driving circuit, separation means being provided between output stage of data signal line driving circuit and data signal line and scanning signal line driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both of a data signal line to be scanned first and a data signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair by referencing Figs. 1 and 2, references t1 and t2, 101 and 102; page 3, paragraph 0017; Fig. 1, reference 102; Figs. 1 and 2, references 101 and 102; and page 2, paragraphs 0014 and 0017. According to the Examiner, it would have been obvious to one of ordinary skill in the art at the time of the invention to use separation means for separating an output stage of data signal line driving circuit from a data signal line in a first half of a selection-scanning period of each scanning signal line by a scanning line driving circuit separation means being provided between output stage of data signal line driving circuit and data signal line and scanning signal line

driving circuit carries out a selection-scanning operation by switching polarities of voltages for gradation display, with respect to both a data signal line to be scanned first and a data signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair as shown by Masami et al. in Udo et al. apparatus in order to reduce power consumption.

Applicants respectfully submit that neither Udo et al. nor Masami et al. taken singly or in combination (assuming these teachings may be combined, which Applicants do not admit), teach or suggest all the claimed limitations of the present invention. Among other things, the references do not disclose the scanning signal line driving circuit carrying out a selection scanning operation by switching polarities of voltages for gradation display, with respect to both of a scanning signal line to be scanned first and a scanning signal line to be scanned next of a pair, in a first half of the selection-scanning period of the scanning signal line to be scanned first of the pair.

Masami et al. do not cure the deficiencies of Udo et al. Masami et al. merely disclose a short-circuit switch 101 provided in the signal line driver LSI (liquid crystal driving device) of the liquid crystal display, and all the data signal lines are short-circuited by setting ON the short-circuit switch 101 in the state where a separation switch 102 is set OFF in the horizontal blanking period.

The teachings of Masami et al. is not sufficient to teach or suggest the scanning signal line driving circuit carrying out a selection scanning operation by switching polarities of voltages for gradation display, with respect to both of a scanning signal line to be scanned first and a scanning signal line to be scanned next of a pair, in a first half of the

selection-scanning period of the scanning signal line to be scanned first of the pair, as recited in claim 7. Masami et al. merely discloses a technique of neutralizing changes between adjacent signal lines by setting ON the short-circuit switch in the blanking period. Changes between different data signal lines, to which adjacent pixels in the scanning signal line direction are respectfully connected, are neutralized.

As such, Masami et al. fails to cure the deficiencies of the teachings of Udo et al.

Applicants respectfully submit that neither Udo et al. nor Masami et al. taken singly or in combination (assuming these references are combinable, which Applicants do not admit) disclose or teach claim 7, and the rejection of claim 7 should be withdrawn.

Applicants also submit that independent claim 8, which discloses a scanning signal line driving circuit carrying out a selection scanning operation by switching polarities of voltages for gradation display, with respect to both of a scanning signal line to be scanned first and a scanning signal line to be scanned next in a pair, in the blanking period directly before the selection-scanning period of the scanning signal line to be scanned first of the pair is distinguishable over the prior art and allowable for at least the same reasons given above with regards to claim 7. Therefore the rejection of claim 8 should be withdrawn.

Applicants also submit that independent claim 12, which discloses "said scanning signal line driving circuit carries out selection scanning with respect to a scanning signal line of a pixel to be scanned first together with a scanning signal line of a pixel to be scanned next of said pair of adjacent pixels in the direction of data signal lines before applying the voltages for display to the pixel to be scanned first of said pair

of adjacent pixels when scanning in switching polarities of the voltages for display" is allowable over the art cited for the reasons set forth above with regard to claim 7.

Applicants also respectfully submit that the Examiner has failed to establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or to combine the reference teachings. Second, the proposed modification of the prior art must have had a reasonable expectation of succeeding, as determined from the vantage point of a skill artisan at the time the invention was made. Third, the prior art references, when combined, must teach or suggest all the claim limitations. *See* M.P.E. P. §2143.

In view of the above reasons, Applicants respectfully submit that the asserted combination of Udo et al. and Masami et al. fail to establish a *prima facie* case of obviousness of independent claims 7, 8 and 12, or any claim depending there from.

By this amendment, Applicants have added new claim 14. It is respectfully submitted that claim 14 is allowable for the reasons set forth above with regard to claim 1 as claim 14 similarly recites "short-circuit means for short-circuiting respective pixel capacitors in the liquid crystal panel of said pair of adjacent pixels in a non-selection period directly before a selection-scanning period of a target scanning signal line when scanning by switching polarities of the voltages for gradation display."

Conclusion

All rejections raised in the Office Action having been addressed, it is respectfully submitted that the present application is in condition for allowance and such allowance is respectfully solicited. Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Demetra R. Smith-Stewart (Reg. No. 47,354), to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1. 17; particularly, extension of time fees.

Respectfully submitted,

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